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NTE5437 & NTE5438
Silicon Controlled Rectifier (SCR)
8 Amp Senstitive Gate, TO220

Description:

The NTE5437 and NTE5438 are silicon controlled rectifiers (SCR) in a TO220 type package designed for general purpose high voltage applications where gate sensitivity is required.

Absolute Maximum Ratings: (T_A = +25°C unless otherwise specified)

Repetitive Peak Off–State Voltage (T_J = –40° to +125°C, R_{GK} = 1kΩ), V_{DRM}, V_{RRM}
- NTE5437 . . . . . 400V
- NTE5438 . . . . . 600V

On–State Current (All Conducting Angles, T_C = +85°C), $I_{T(RMS)}$ 8A

Average On–State Current (Half Cycle, ⊖ = 180°, T_C = +85°C), $I_{T(AV)}$ 5.1A

Non–Repetitive On–State Current, I_{TSM}
- Half Cycle, 60Hz 88A
- Half Cycle, 50Hz 80A

Fusing Current (t= 10ms, Half Cycle), I^2t . . . . . $32A^2s$

Peak Reverse Gate Voltage (I_{GR} = 50μA), V_{GRM} 8V

Peak Gate Current (10μs Max), I_{GM} 2A

Peak Gate Dissipation (10μs Max), P_{GM} 5W

Gate Dissipation (20ms Max), $P_{G(AV)}$ 0.5W

Oprating Junction Temperature Range, T_J . . . . . –40° to +125°C

Storage Temperature Range, T_{stg} . . . . . –40° to +125°C

Lead Temperature (During Soldering, 1.6mm from case, 10sec Max), T_L . . . . . +250°C

Thermal Resistance, Junction–to–Case, R_{thJC} 4K/W

Thermal Resistance, Junction–to–Ambient, R_{thJA} 60K/W

Electrical Characteristics: (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Off–State Leakage Current	I_{DRM}, I_{RRM}	V_{DRM} + V_{RRM} = Rated Voltage, R_{GK} = 1kΩ	T_J = +125°C	–	0.5	mA
			T_J = +25°C	–	5.0	μA

Electrical Characteristics (Cont'd): (T_A = +25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Max	Unit
On−State Voltage	V_T	I_T = 16A, T_J = +25°C	–	1.95	V
On−State Threshold Voltage	$V_{T(TO)}$	T_J = +125°C	–	1.05	V
On−State Slope Resistance	r_T	T_J = +125°C	–	65	mΩ
Gate Trigger Current	I_{GT}	V_D = 7V	–	200	μA
Gate Trigger Voltage	V_{GT}	V_D = 7V	–	2.0	V
Holding Current	I_H	R_{GK} = 1kΩ	–	10	mA
Latching Current	I_L	R_{GK} = 1kΩ	–	20	mA
Critical Rate of Voltage Rise	dv/dt	V_D = .67 x V_{DRM}, R_{GK} = 1kΩ, T_J = +125°C	5	–	V/μs
Critical Rate of Current Rise	di/dt	I_G = 10mA, di_G/dt = 0.1A/μs, T_J = +125°C	100	–	A/μs
Gate Controlled Delay Time	t_{gd}	I_G = 10mA, di_G/dt = 0.1A/μs	–	500	ns
Commutated Turn−Off Time	t_q	T_C = +85°C, V_D = .67 x V_{DRM}, V_R = 35V, I_T = 5.1A	–	100	μs