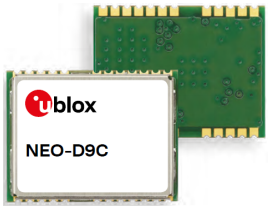
NEO-D9C-00B

QZSS correction service receiver

Professional grade

Data sheet



Abstract

This data sheet describes the NEO-D9C QZSS L6 receiver for CLAS and MADOCA. This NEO form factor module provides easy integration of QZSS augmentation services and enables GNSS receivers to reach cm-level accuracies.

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Document information

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Product status	Corresponding content status	
Functional Sample	Draft	For functional testing. Revised and supplementary data will be published later.
In development / prototype	Objective specification	Target values. Revised and supplementary data will be published later.
Engineering sample	Advance information	Data based on early testing. Revised and supplementary data will be published later.
Initial production	Early production information	Data from product verification. Revised and supplementary data may be published later.
Mass production / End of life	Production information	Document contains the final product specification.

This document applies to the following products:

Product name	Type number	FW version	IN/PCN reference	Product status
NEO-D9C	NEO-D9C-00B-02	QZS 1.01	UBX-22003112 UBX-22039049	Mass production

Contents

1 Functional description

1.1 Overview

NEO-D9C-00B is a QZSS L6 receiver that brings QZSS Centimeter Level Augmentation Service (CLAS) support to u-blox GNSS modules, enabling centimeter-level navigation. The receiver can also track the experimental MADOCA service transmitted on the QZSS L6 signal.

When combined with other u-blox products, the NEO-D9C-00B can be used to build a complete and stand-alone high precision system providing users with access to free high accuracy correction services and ultimately centimeter-level GNSS accuracy.

1.2 Performance

Parameter		Specification
Receiver type		u-blox D9 engine QZSS L2C and L6 receiver

QZSS L2C and L6		Specification
Time to first frame [1]		Hot start 3 s, Cold start 18 s
Decoding sensitivity [2]		90% frame rate at -136 dBm
Acquisition sensitivity [3]		Hot start: -154 dBm, Cold start: -137 dBm
Specification compliance		PS-QZSS-001
Number of concurrent L6 reception channels		2
Frequency range		1227.60 MHz +/- 5 MHz and 1278.75 MHz +/- 5 MHz
Communication interface		UART/USB/I2C/SPI
Communication speed		Up to 921600 baud UART, USB 2.0, SPI 125 kB/s, I2C 400 kbit/s
Vehicle dynamics	Dynamics	≤ 4 g
	Velocity	500 m/s

Table 1: u-blox NEO-D9C-00B performance

1.3 Supported GNSS augmentation systems

1.3.1 Quasi-Zenith Satellite System (QZSS)

The Quasi-Zenith Satellite System (QZSS) is a Japanese satellite positioning system. With satellites in quasi-zenith orbits, three satellites will be visible at all times from locations in the Asia-Oceania region. The QZSS correction stream is provided on the L6 band for free.

Signal	QZS1	QZS2/4	QZS3	Service	Frequency
Orbit	QZO	QZO	GEO		
L2C	Transmit	Transmit	Transmit	PNT	1227.60 MHz
L6	L6D	L6D/L6E	L6D/L6E	CLAS/MADOCA	1278.75 MHz

Table 2: QZSS satellites and signals

1 With ZED-F9P aiding messages provided, open sky conditions from QZS-1

2 Power with respect to single component L6D/L6E using a 20-25 dB external LNA

3 Success rate of acquiring at least one L2 QZSS signal > 95% using constellation of 4 visible QZSS satellites using a 20-25 dB external LNA

☞ QZS1 only transmits the CLAS L6D message, while QZS2, QZS3 and QZS4 transmit both CLAS L6D and MADOCA L6E messages.

1.4 Supported protocols

The NEO-D9C-00B supports the following protocols:

Protocol	Type
UBX	Input/output, binary, u-blox proprietary

Table 3: Supported protocols

For specification of the protocols, see the Interface description [2].

2 System description

2.1 Block diagram

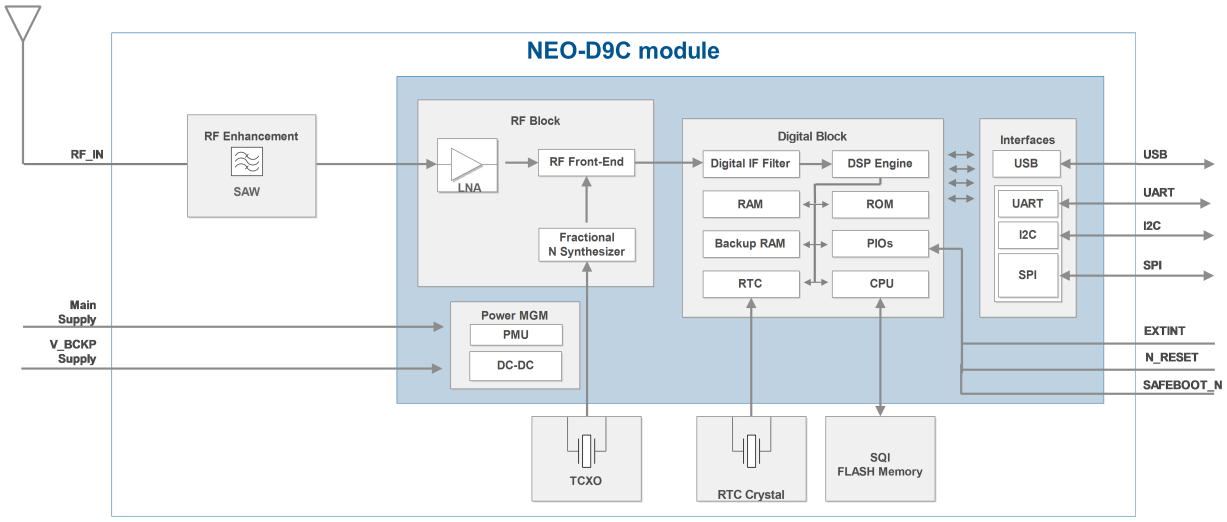

Figure 1: NEO-D9C-00B block diagram

An active antenna is mandatory with the NEO-D9C-00B.

3 Pin definition

3.1 Pin assignment

The pin assignment of the NEO-D9C-00B module is shown in Figure 2. The defined configuration of the PIOs is listed in Table 4.

☞ V_BCKP functionality (pin 22: Reserved), ANT_OFF, ANT_DETECT, ANT_SHORT_N are not available.

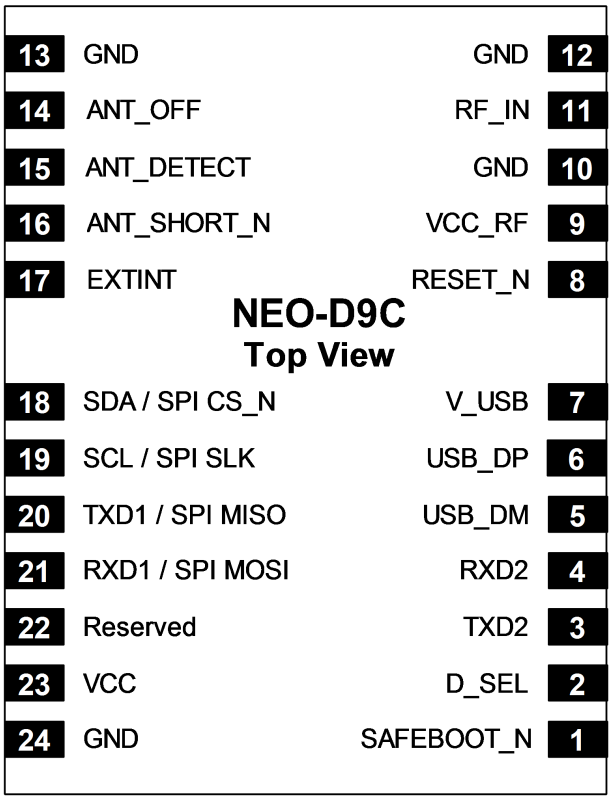

Figure 2: NEO-D9C-00B pin assignment

Pin no.	Name	I/O	Description
1	SAFEBOOT_N	I	SAFEBOOT_N (used for FW updates and reconfiguration, leave open)
2	D_SEL	I	UART 1 / SPI select. (open or high = UART 1)
3	TXD2	O	UART 2 TXD
4	RXD2	I	UART 2 RXD
5	USB_DM	I/O	USB data (DM)
6	USB_DP	I/O	USB data (DP)
7	V_USB	I	USB supply
8	RESET_N	I	RESET (active low)
9	VCC_RF	O	External LNA power
10	GND	I	Ground
11	RF_IN	I	Active antenna L2/L6 band signal input
12	GND	I	Ground

Pin no.	Name	I/O	Description
13	GND	I	Ground
14	ANT_OFF	O	External LNA disable - default active high
15	ANT_DETECT	I	Active antenna detect - default active high
16	ANT_SHORT_N	O	Active antenna short detect - default active low
17	EXTINT	I	External interrupt pin
18	SDA / SPI CS_N	I/O	I2C data if D_SEL = VCC (or open); SPI chip select if D_SEL = GND
19	SCL / SPI SLK	I/O	I2C clock if D_SEL = VCC (or open); SPI clock if D_SEL = GND
20	TXD / SPI MISO	O	UART1 output if D_SEL = VCC (or open); SPI MISO if D_SEL = GND
21	RXD / SPI MOSI	I	UART1 input if D_SEL = VCC (or open); SPI MOSI if D_SEL = GND
22	Reserved	-	No connection
23	VCC	I	Supply voltage
24	GND	I	Ground

Table 4: NEO-D9C-00B pin assignment

☞ For detailed information on the pin functions and characteristics see the integration manual [1].

4 Electrical specification

The limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134).

CAUTION Operating the device above one or more of the limiting values may cause permanent damage to the device. The values provided in this chapter are stress ratings. Extended exposure to the values outside the limits may effect the device reliability.

Where application information is given, it is advisory only and does not form part of the specification.

4.1 Absolute maximum ratings

Parameter	Symbol	Condition	Min	Max	Units
Power supply voltage	VCC		-0.5	3.6	V
Voltage ramp on VCC[4]			20	8000	µs/V
Input pin voltage	Vin		-0.5	VCC + 0.5	V
VCC_RF output current	ICC_RF			100	mA
Supply voltage USB	V_USB		–0.5	3.6	V
USB signals	USB_DM, USB_DP		-0.5	V_USB + 0.5	V
Input power at RF_IN	Prfin	source impedance = 50 Ω, continuous wave		10	dBm
Storage temperature	Tstg		-40	+85	°C

Table 5: Absolute maximum ratings

CAUTION Risk of equipment damage. This product is not protected against overvoltage or reversed voltages. Use appropriate protection diodes to avoid voltage spikes exceeding the specified boundaries damaging the equipment.

4.2 Operating conditions

The values for the following operating conditions have been specified at 25°C ambient temperature. Extreme operating temperatures can significantly impact the specified values. If an application operates near the min or max temperature limits, ensure the specified values are not exceeded.

Parameter	Symbol	Min	Typical	Max	Units	Condition
Power supply voltage	VCC	2.7	3.0	3.6	V	
SW backup current	I_SWBCKP		0.07		mA	
Input pin voltage range	Vin	0		VCC	V	
Digital IO pin low level input voltage	Vil			0.4	V	
Digital IO pin high level input voltage	Vih	0.8 * VCC			V	
Digital IO pin low level output voltage	Vol			0.4	V	Iol = 2 mA
Digital IO pin high level output voltage	Voh	VCC – 0.4			V	Ioh = 2 mA
DC current through any digital I/O pin (except supplies)	Ipin			5	mA	
VCC_RF voltage	VCC_RF		VCC - 0.1		V	
VCC_RF output current	ICC_RF			50	mA	

[4] Exceeding the ramp speed may permanently damage the device

Parameter	Symbol	Min	Typical	Max	Units	Condition
Receiver chain noise figure[5]	NFtot		11		dB	
Recommended LNA gain into module	LNA_gain		20		dB	
Operating temperature	Topr	-40	+25	+85	°C	

Table 6: Operating conditions

☞ Operation beyond the specified operating conditions can affect the device reliability.

4.3 Indicative power requirements

Table 7 provides examples of typical current requirements when using a cold start command. The given values are total system supply current for a possible application including RF and baseband sections.

☞ The actual power requirements vary depending on the FW version used, external circuitry, number of satellites tracked, signal strength, type and time of start, duration, and conditions of test.

Symbol	Parameter	Conditions	QZSS L6	Unit
I_{PEAK}	Peak current	Acquisition & tracking	130	mA
$I_{AVERAGE}$	Average current	Acquisition & tracking	55	mA

Table 7: Currents to calculate the indicative power requirements

All values in Table 7 are measured at 25 °C ambient temperature.

[5] Only valid for the QZSS L2 band

5 Communications interfaces

There are several communications interfaces including UART, SPI, I2C and USB.

5.1 UART

UART1 is the main UART interface for UBX protocol host control and message output.

Symbol	Parameter	Min	Max	Unit
R_u	Baud rate	9600	921600	bit/s
Δ_{Tx}	Tx baud rate accuracy	-1%	+1%	-
Δ_{Rx}	Rx baud rate tolerance	-2.5%	+2.5%	-

Table 8: NEO-D9C-00B UART specifications

5.2 SPI

All the inputs have internal pull-up resistors in normal operation and can be left open if not used. All the PIOs are supplied by VCC, therefore all the voltage levels of the PIO pins are related to VCC supply voltage.

The NEO-D9C-00B has an SPI slave interface that can be selected by setting D_SEL = 0. The SPI pins available are: SPI_MISO (TXD), SPI_MOSI (RXD), SPI_CS_N, SPI_CLK. The SPI interface is designed to allow communication to a host CPU. The interface can be operated in slave mode only. Note that SPI is not available in the default configuration because its pins are shared with the UART1 and I2C interfaces. The maximum transfer rate using SPI is 125 kB/s and the maximum SPI clock frequency is 5.5 MHz.

This section provides SPI timing values for the NEO-D9C-00B slave operation. The following tables present timing values under different capacitive loading conditions. Default SPI configuration is CPOL = 0 and CPHA = 0.

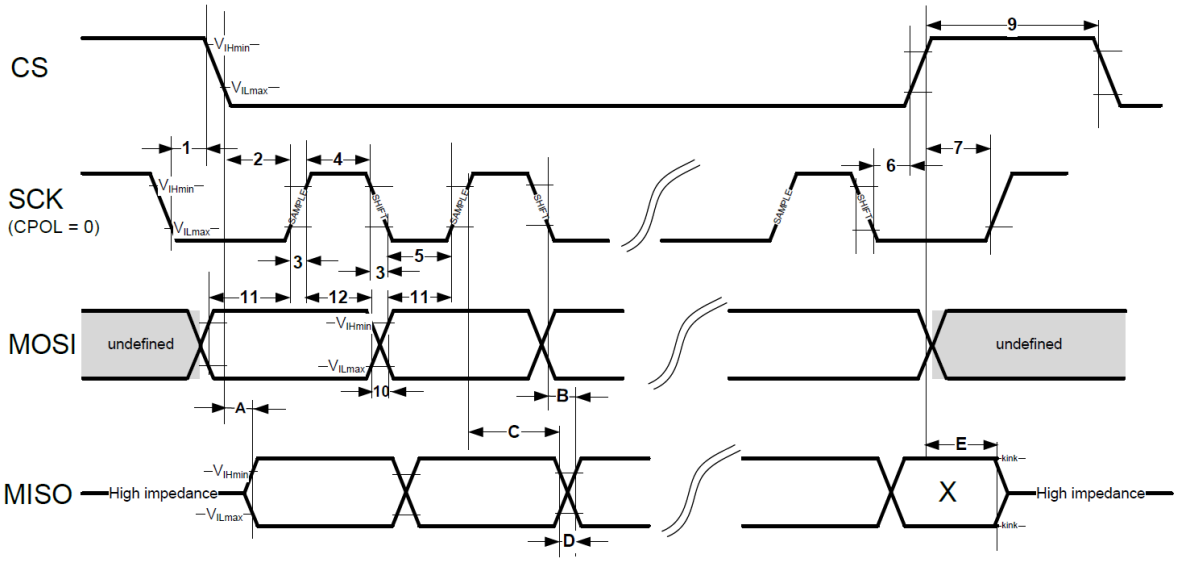

Figure 3: NEO-D9C-00B SPI specification mode 1: CPHA=0 SCK = 5.33 MHz

Timings 1 - 12 are not specified here.

Timing value at 2 pF load	Min (ns)	Max (ns)
"A" - MISO data valid time (CS)	14	38
"B" - MISO data valid time (SCK) weak driver mode	21	38
"C" - MISO data hold time	114	130
"D" - MISO rise/fall time, weak driver mode	1	4
"E" - MISO data disable lag time	20	32

Table 9: NEO-D9C-00B SPI timings at 2pF load

Timing value at 20 pF load	Min (ns)	Max (ns)
"A" - MISO data valid time (CS)	19	52
"B" - MISO data valid time (SCK) weak driver mode	25	51
"C" - MISO data hold time	117	137
"D" - MISO rise/fall time, weak driver mode	6	16
"E" - MISO data disable lag time	20	32

Table 10: NEO-D9C-00B SPI timings at 20pF load

Timing value at 60 pF load	Min (ns)	Max (ns)
"A" - MISO data valid time (CS)	29	79
"B" - MISO data valid time (SCK) weak driver mode	35	78
"C" - MISO data hold time	122	152
"D" - MISO rise/fall time, weak driver mode	15	41
"E" - MISO data disable lag time	20	32

Table 11: NEO-D9C-00B SPI timings at 60pF load

5.3 I2C

An I2C compliant interface is available for communication with an external host CPU. The interface can be operated in slave mode only. It is fully compatible with Fast-mode of the I2C industry standard. Since the maximum SCL clock frequency is 400 kHz, the maximum bit rate is 400 kbit/s. The interface stretches the clock when slowed down while serving interrupts, therefore the real bit rates may be slightly lower.

☞ The I2C interface is only available with the UART default mode. If the SPI interface is selected by using D_SEL = 0, the I2C interface is not available.

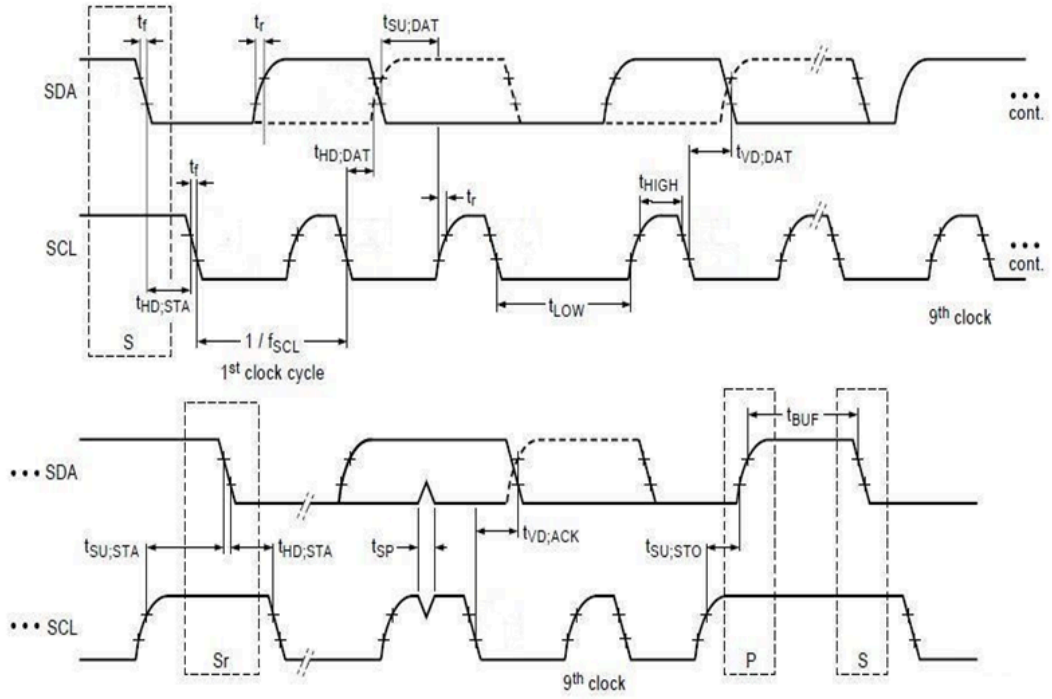

Figure 4: NEO-D9C-00B I2C slave specification

Symbol	Parameter	Min (Standard / Fast-mode)	Max	Unit
f_{SCL}	SCL clock frequency	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition	4.0/1	-	µs
t_{LOW}	Low period of the SCL clock	5/2	-	µs
t_{HIGH}	High period of the SCL clock	4.0/1	-	µs
$t_{SU;STA}$	Setup time for a repeated START condition	5/1	-	µs
$t_{HD;DAT}$	Data hold time	0/0	-	µs
$t_{SU;DAT}$	Data setup time	250/100		ns
t_r	Rise time of both SDA and SCL signals	-	1000/300 (for C 400pF)	ns
t_f	Fall time of both SDA and SCL signals	-	300/300 (for C 400pF)	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0/1	-	µs
t_{BUF}	Bus-free time between a STOP and START condition	5/2	-	µs
$t_{VD;DAT}$	Data-valid time	-	4/1	µs
$t_{VD;ACK}$	Data-valid acknowledge time	-	4/1	µs
V_{nL}	Noise margin at the low level	0.1 VCC	-	V
V_{nH}	Noise margin at the high level	0.2 VCC	-	V

Table 12: NEO-D9C-00B I2C slave timings and specifications

5.4 USB

The USB 2.0 FS (Full Speed, 12 Mbit/s) interface can be used for host communication. Due to the hardware implementation, it may not be possible to certify the USB interface. The V_USB pin supplies the USB interface.

5.5 Default interface settings

Interface	Settings
UART	9600 baud, 8 bits, no parity bit, 1 stop bit. Output protocol: UBX. Only the following UBX message (if enabled) will be output if there is valid data: **UBX-RXM-QZSSL6**. Input protocols without need of additional configuration: UBX.
USB	Output messages activated as in UART. Input protocols available as in UART.
I2C	Output messages activated as in UART. Input protocols available as in UART.
SPI	Output messages activated as in UART. Input protocols available as in UART.

Table 13: Default interface settings

☞ The boot message is still output using $GNTXT messages. The messages are output when the NEO-D9C-00B is powered up.

☞ Refer to the applicable interface description [2] for information about further settings.

6 Mechanical specification

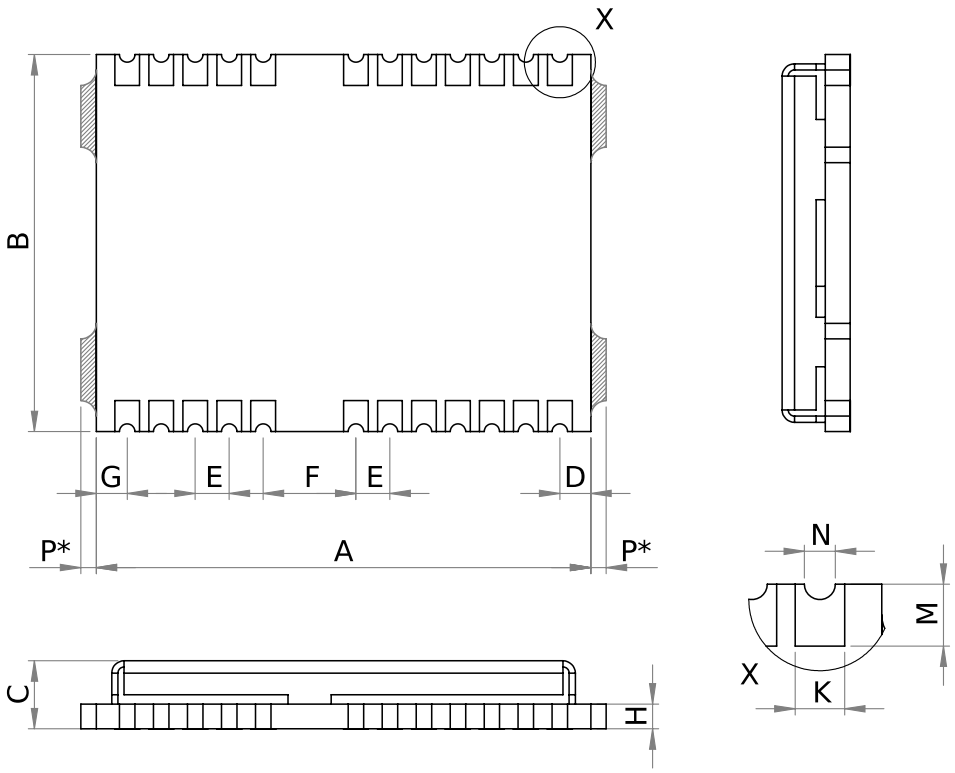

Figure 5: NEO-D9C-00B mechanical drawing

Symbol	Min (mm)	Typical (mm)	Max (mm)	
A	15.9	16.0	16.1	
B	12.1	12.2	12.3	
C	2.2	2.4	2.6	
D	0.9	1.0	1.1	
E	1.0	1.1	1.2	
F	2.9	3.0	3.1	
G	0.9	1.0	1.1	
H	-	0.82	-	
K	0.7	0.8	0.9	
M	0.8	0.9	1.0	
N	0.4	0.5	0.6	
P*	0.0	-	0.5	The de-paneling residual tabs may be on either side (not both).
Weight		1.6 g		

Table 14: NEO-D9C-00B mechanical dimensions

☞ The mechanical picture of the de-paneling residual tabs (P*) is an approximate representation, shape and position may vary.

☞ Component keep-out area must consider that the de-paneling residual tabs can be on either side (not both).

7 Reliability tests

NEO-D9C-00B modules are based on AEC-Q100 qualified GNSS chips.

Tests for product family qualifications are according to ISO 16750 "Road vehicles – environmental conditions and testing for electrical and electronic equipment" , and appropriate standards.

8 Labeling and ordering information

This section provides information about product labeling and ordering. For information about moisture sensitivity level (MSL), product handling and soldering see the Integration manual [1].

8.1 Product labeling

The labeling of the NEO-D9C-00B modules provides product information and revision information. For more information contact u-blox sales.

8.2 Explanation of product codes

Three product code formats are used in the NEO-D9C-00B labels. The **Product name** used in documentation such as this data sheet identifies all u-blox products, independent of packaging and quality grade. The **Ordering code** includes options and quality, while the **Type number** includes the hardware and firmware versions.

Table 15 below details these three formats.

Format	Structure	Product code
Product name	PPP-TGV	NEO-D9C
Ordering code	PPP-TGV-NNQ	NEO-D9C-00B
Type number	PPP-TGV-NNQ-XX	NEO-D9C-00B-02

Table 15: Product code formats

The parts of the product code are explained in Table 16.

Code	Meaning	Example
PPP	Product family	NEO
TG	Platform	D9 = u-blox D9
V	Variant	C = QZSS corrections
NNQ	Option / Quality grade	NN: Option [00...99] Q: Grade, A = Automotive, B = Professional
XX	Product detail	Describes hardware and firmware versions

Table 16: Part identification code

8.3 Ordering codes

Ordering code	Product	Remark
NEO-D9C-00B	NEO-D9C	u-blox D9 correction module QZSS L6 receiver for CLAS and MADOCA service

Table 17: Product ordering codes

☞ Product changes affecting form, fit or function are documented by u-blox. For a list of Product Change Notifications (PCNs) see our website at: https://www.u-blox.com/en/product-resources.

Related documents

[1] NEO-D9C Integration manual, UBX-21031631

[2] QZS 1.01 Interface description, UBX-21031777

☞ For regular updates to u-blox documentation and to receive product change notifications please register on our homepage https://www.u-blox.com.

Revision history

Revision	Date	Name	Status / comments
R01	15-Sep-2017	ghun/jhak	Draft
R02	29-Sep-2017	ghun/jhak	Draft / updated pins 15 and 16
R03	29-Apr-2019	ghun	Objective Specification
R04	23-May-2019	ghun	Advance Information
R05	27-June-2019	ghun	Early Production Information - V_BCKP not used
R06	25-Mar-2020	jhak/ghun	PCN UBX-19057484 added and module type number updated. Absolute maximum ratings and Operating conditions tables updated.
R07	27-Oct-2020	dama	USB interface section update. UART interface section update. SW backup current update
R08	15-Sep-2021	dbhu	Update average current value. firmware QZS 1.01 update.
R09	17-Dec-2021	dama	Overall text improvement and typo corrections. Disclosure restriction C1-Public
R10	09-Feb-2022	dama	Production information
R11	16-Dec-2022	dbhu	Overall text improvement Updated the section Mechanical specification

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